

# CNR-INFM - Perugia Unit

## Activity under FP6 - DETNI Project

### Development of a neutron detector based on Silicon Micro-Strip technology

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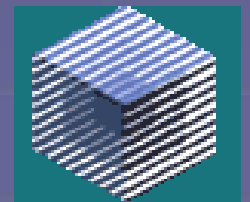
#### Summary

- Overview of the past activity
- Design and realization
- Preliminary tests
- Further steps



In the Joint Research Activity DETNI (DETEctors for Neutron Instrumentation), of the Integrated Infrastructure Initiative for Neutron Scattering and Muon Spectroscopy (NMI3) in the EU Research Framework Programme FP6, **three prototypes of novel modular thermal neutron area detector** were developed, together with the necessary novel and very modern readout and data acquisition technology.

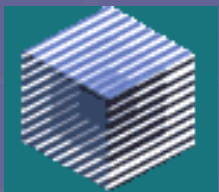
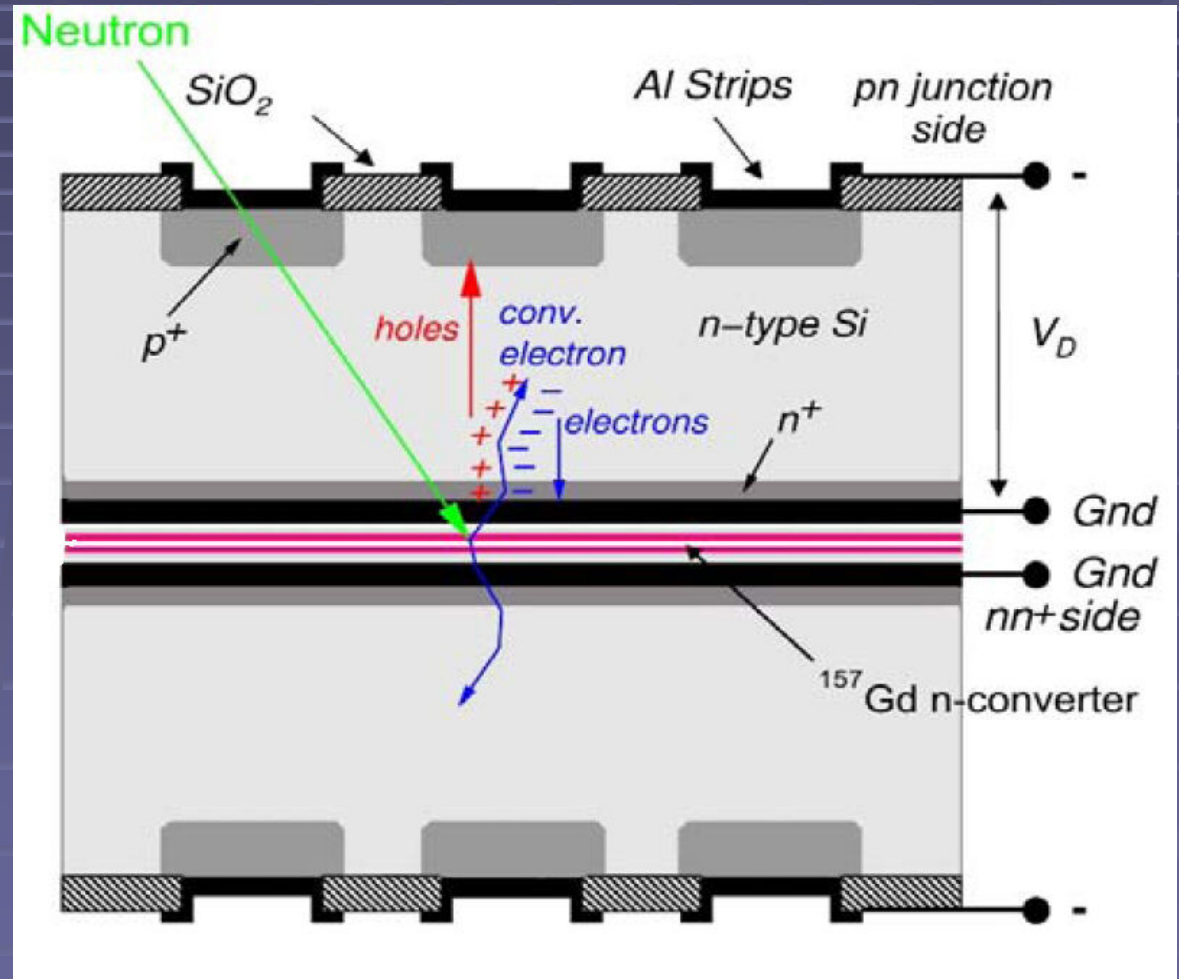
Perugia's group, in particular, worked on a **two-dimensional position sensitive detector** made of two double-sided Silicon Micro-strip Detectors (Si-MSD) with central  **$^{157}\text{Gd}$**  thin solid neutron converter.



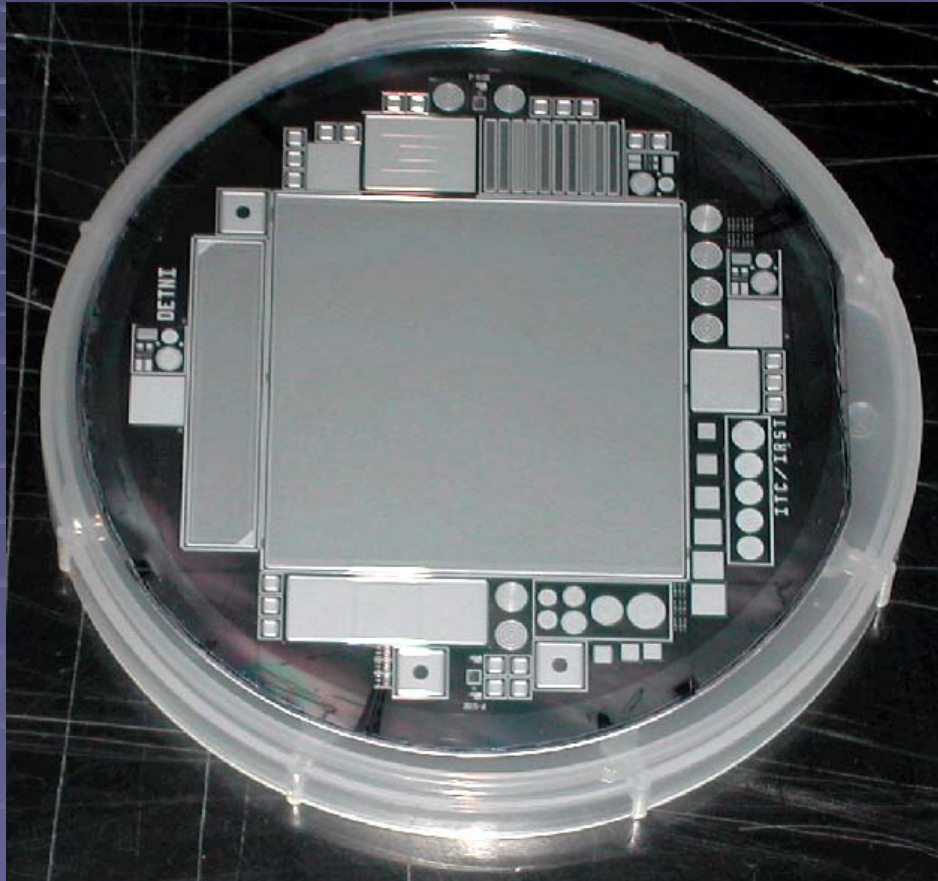
# Basic Idea



- A neutron hits the converter
- Conversion electrons cross the Si-MSD generating electron-hole pairs
- The charge is collected by the strips



Specific **silicon sensors** have been developed

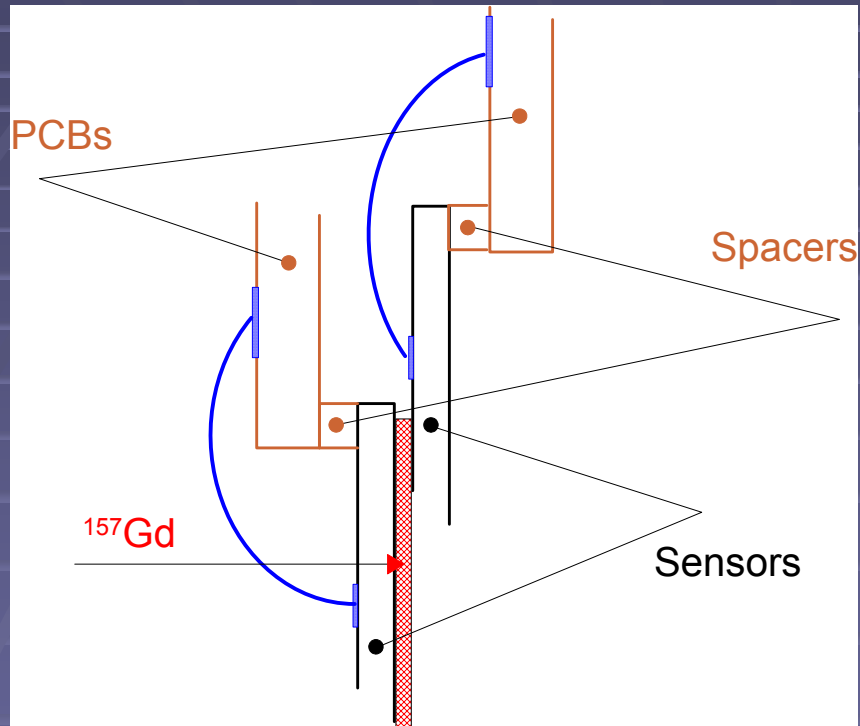


The silicon sensor developed has a dimension of about **53x53 mm**; p+ and n+ planes have 640 orthogonal strips with **80  $\mu\text{m}$  pitch**.

Each strip has AC and DC pads on both ends.



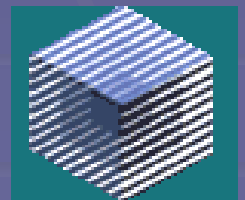
# Sensors stacking: How to?



In order to make bonds on both sides of both silicon sensors using wire bond, a sensor shift is needed.

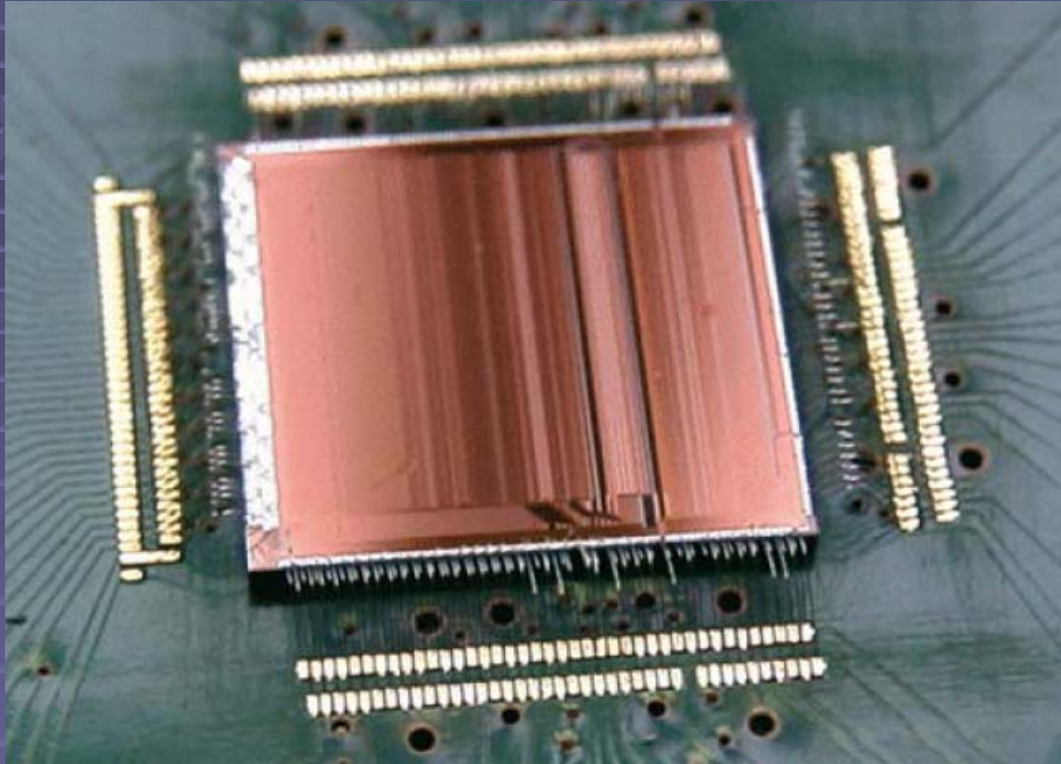
The shown solution has been developed.

Several constraints (short border, minimum bond height, ...) made the mechanical system a critical point, to be accurately developed.





# Application Specific Integrated Circuit



Because of strict requirements of the detector an application specific integrated circuit (ASIC) has been developed at Heidelberg with the collaboration of Perugia's group. The ASIC, called n-XYTER, is a 128-channel chip with high timing-resolution,

time stamp generator, digital/analog output, 256 MHz clock, I2C slow control.



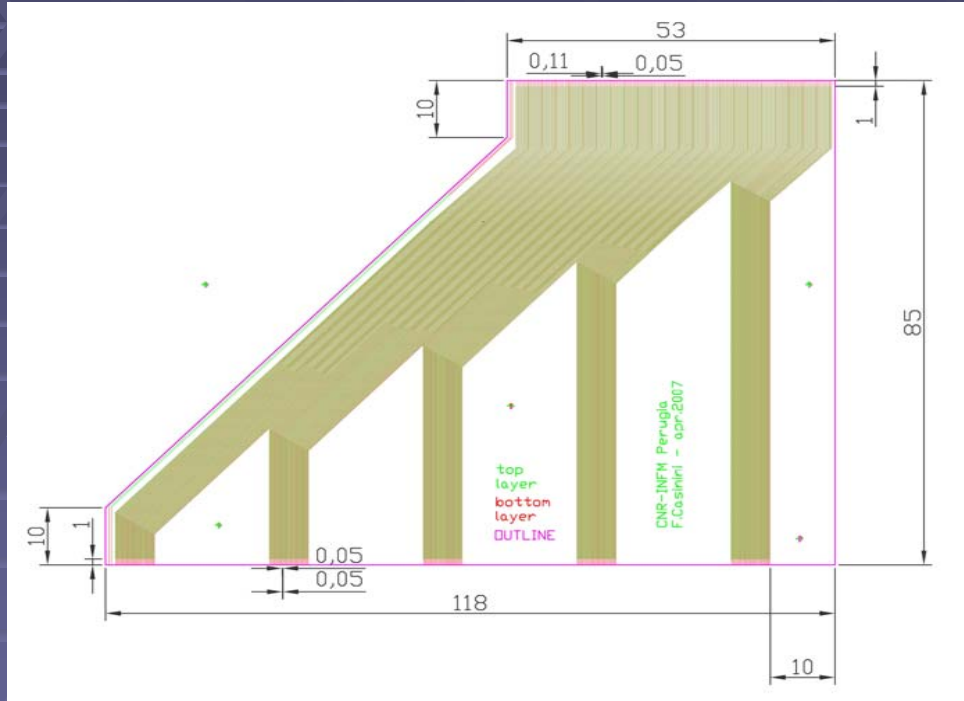
# ASIC features



- process: AMS 0.35  $\mu\text{m}$  CMOS
- 128 channels @ 50.7  $\mu$  pitch
- freely running, self triggered autonomous hit detection
- dynamic range for 6 MIPs
- Shaping time and noise performance:
  - 30 ns fast shaper at 30 pF input, 850 enc for positive signals, 1000 enc for negative signals
  - 130 ns slow shaper at 30 pF input, 600 enc
- digital (time stamp+ch.no.) + analog output
- Timing resolution  $\sim$  2-3 ns, time stamp resolution 1 ns
- positive and negative signals
- local threshold adjustment



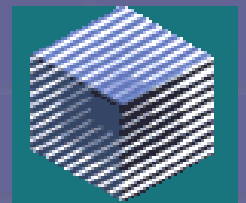
# Physical interface with readout electronics



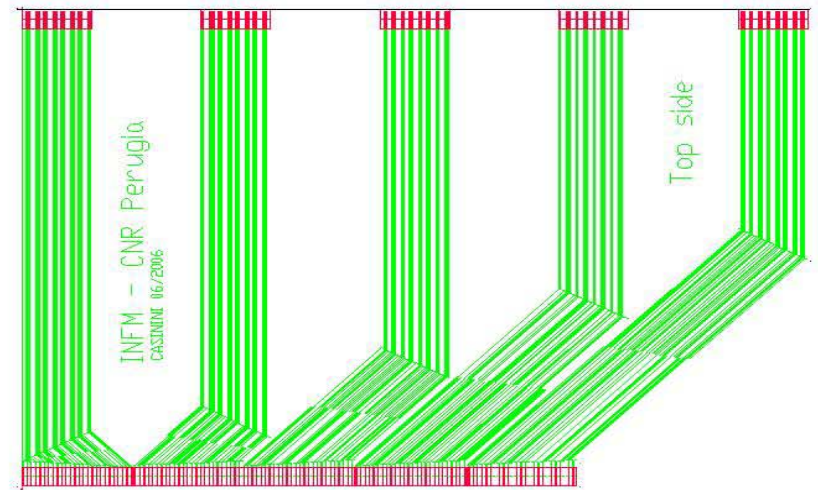
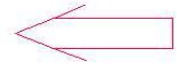
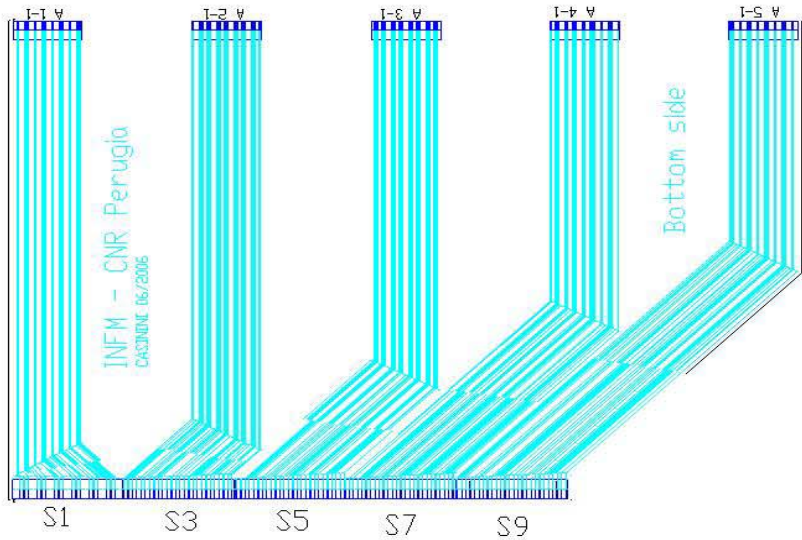
Actual (2007) production technology doesn't permit to obtain reliable rigid/flexible printed circuits with sensor pitch ( $80\mu\text{m}$ ).

A multilayer (flexible) printed circuit is needed to connect the front-end electronics.

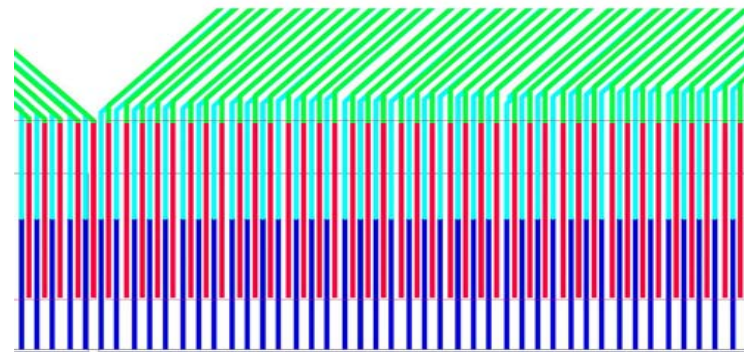
FPC required two different layouts since it was impossible for Cicorel to produce good samples on first batch



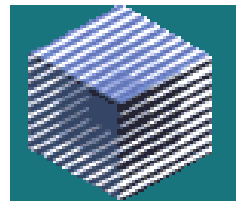




Two flexible printed circuits (kapton) were stacked and aligned achieving the desired result.

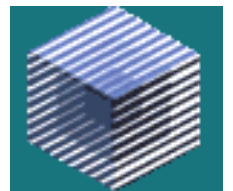
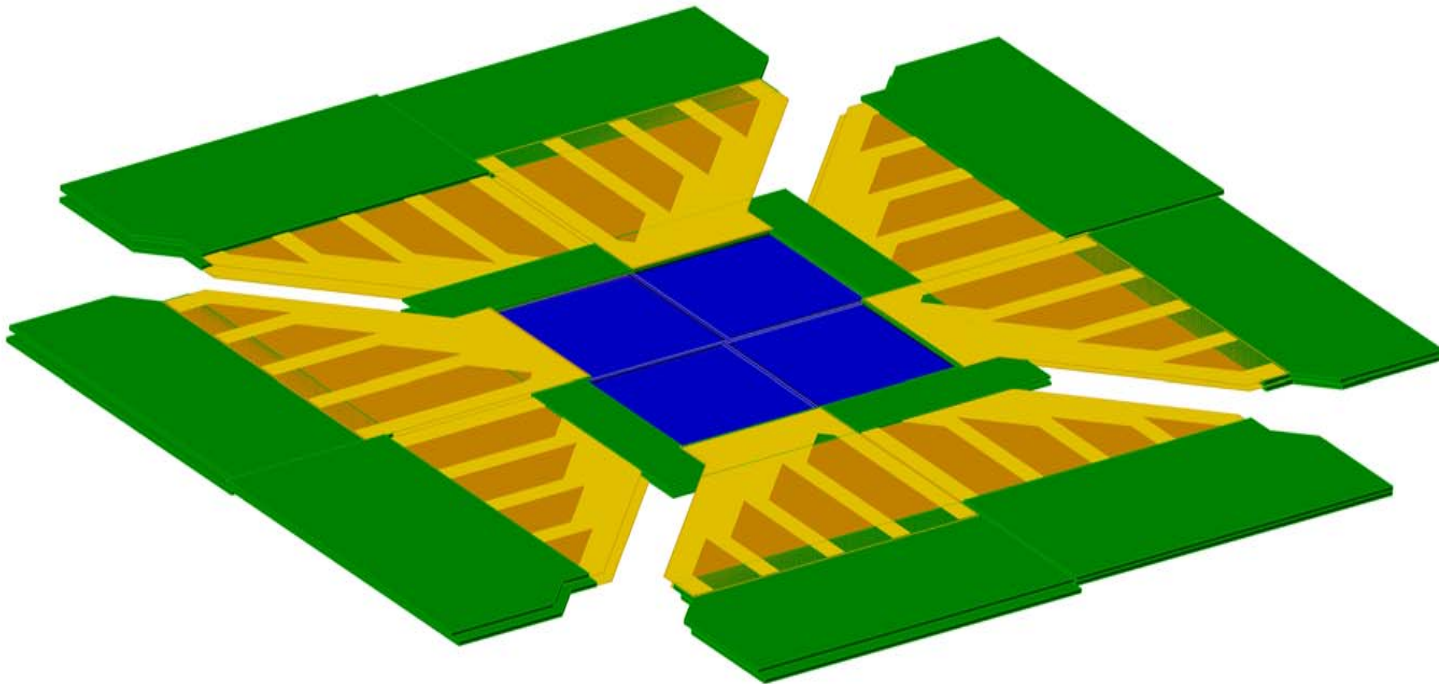


Detail of stacked FPCs



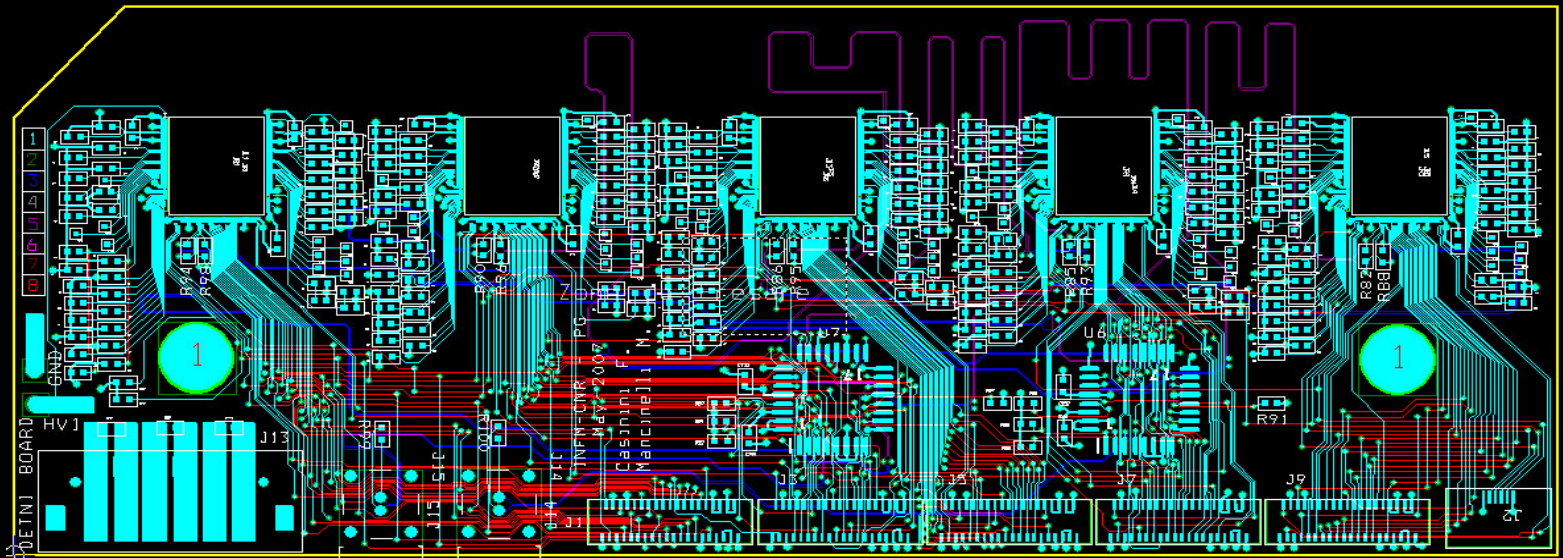
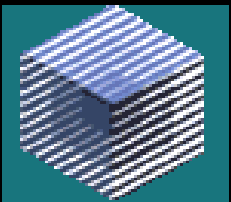
# Front-end electronics: How to?

In the original project, the final detector was made of 4 juxtaposed couples of stacked silicon sensors; this idea required also a particular design for the front-end electronics.



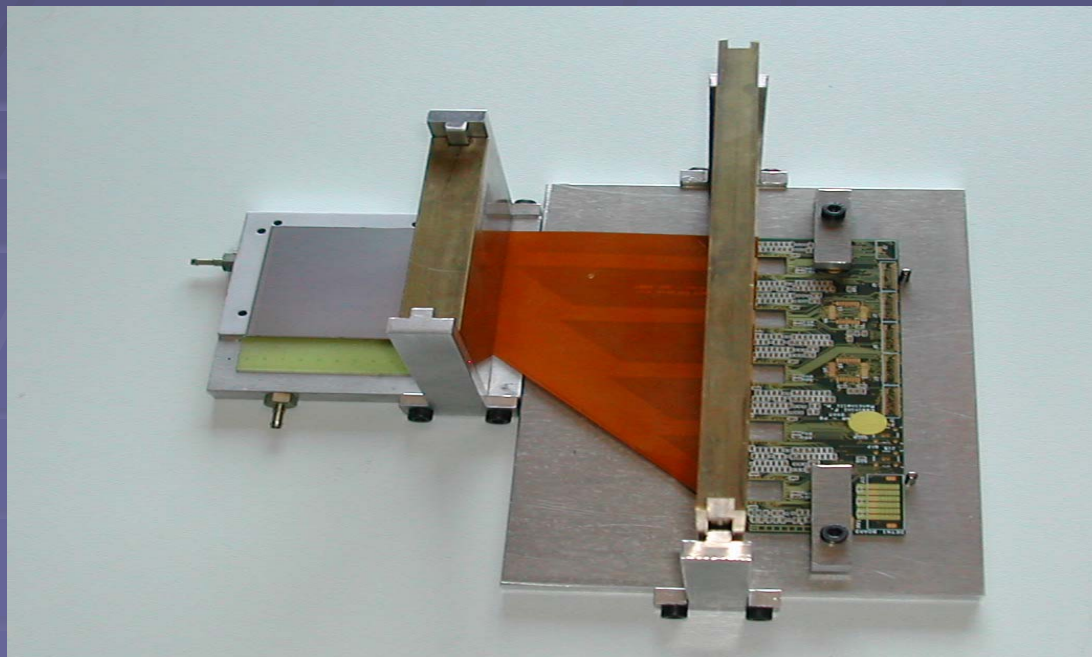
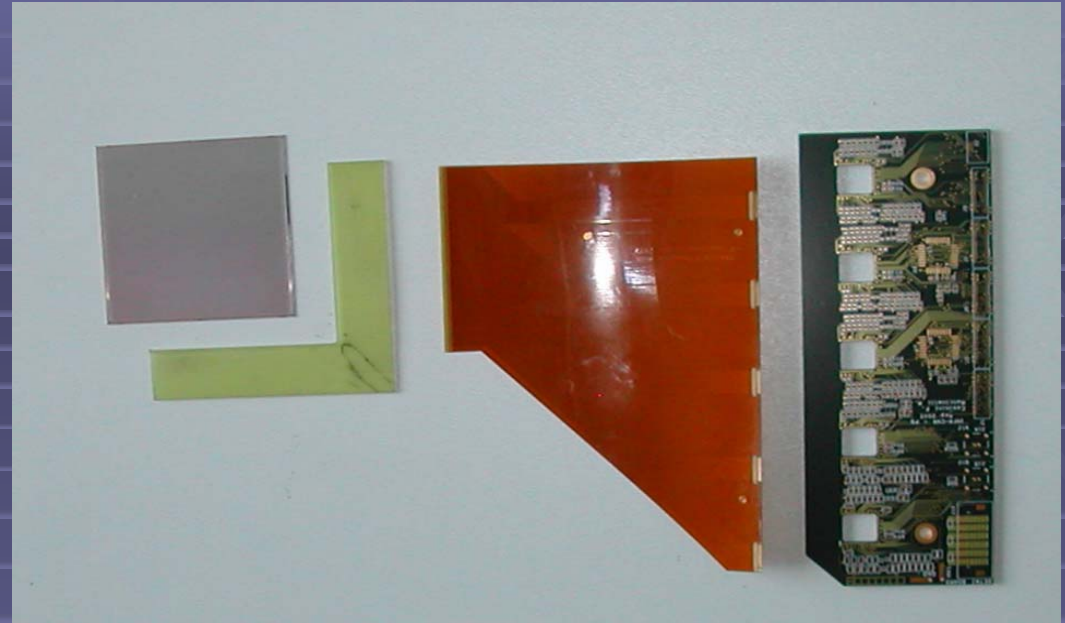
# Front-end electronics

Taking care of physical constraint of the whole system and in consideration of the strong thermal requirement of the novel readout ASIC, an 8 layer 130x50 mm PCB was designed and produced.

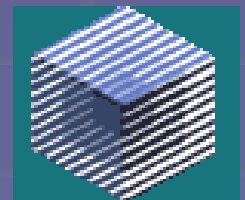




# Mechanical solutions

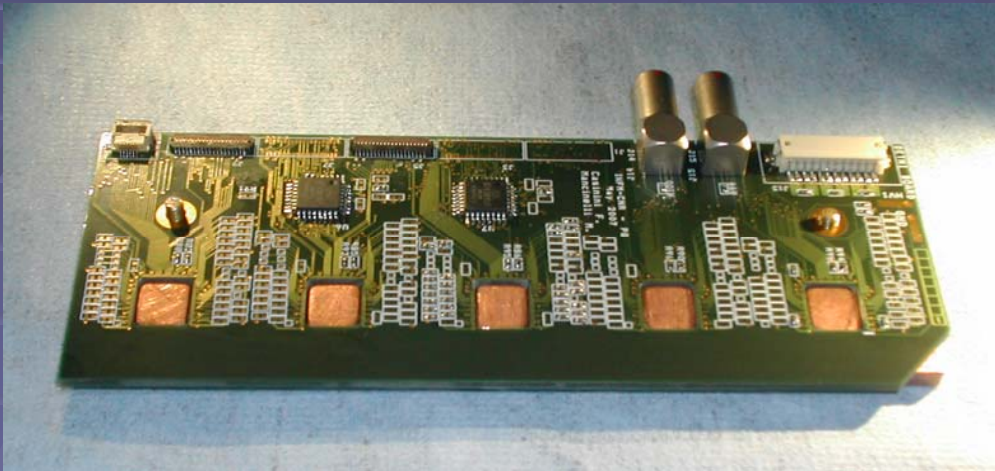
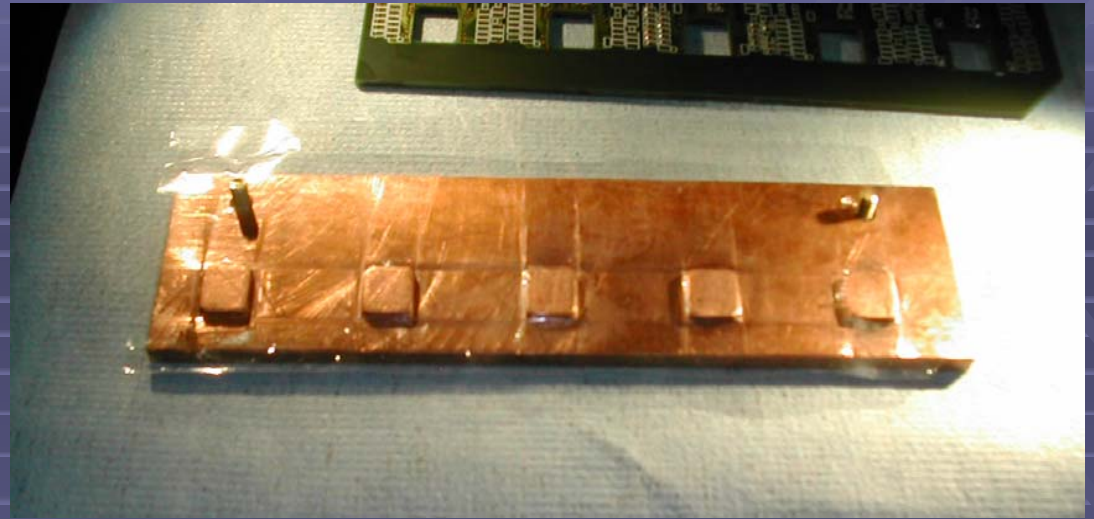


First prototype  
assembly phases



# Thermal issues

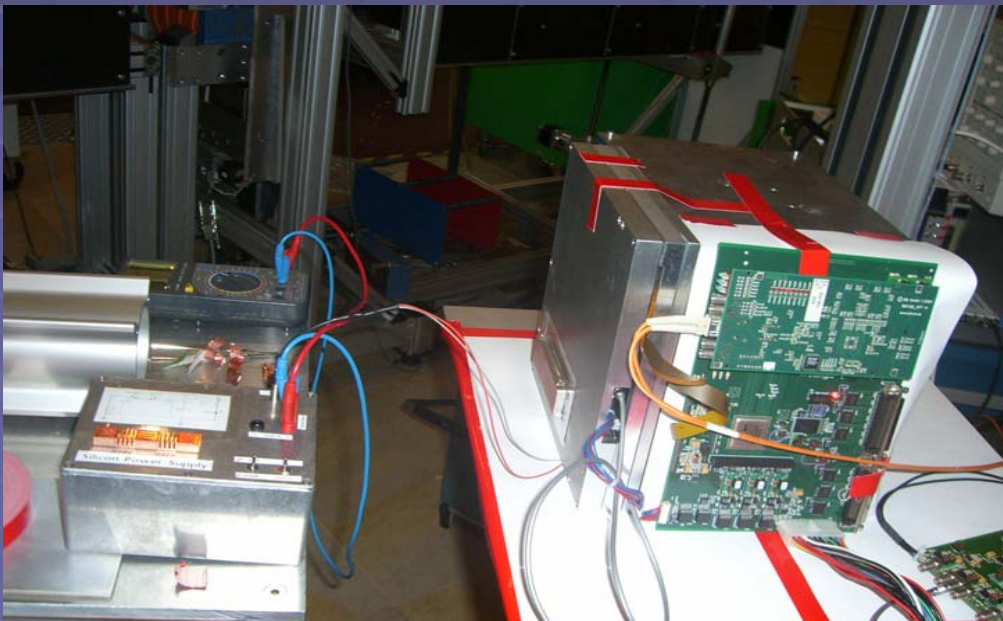
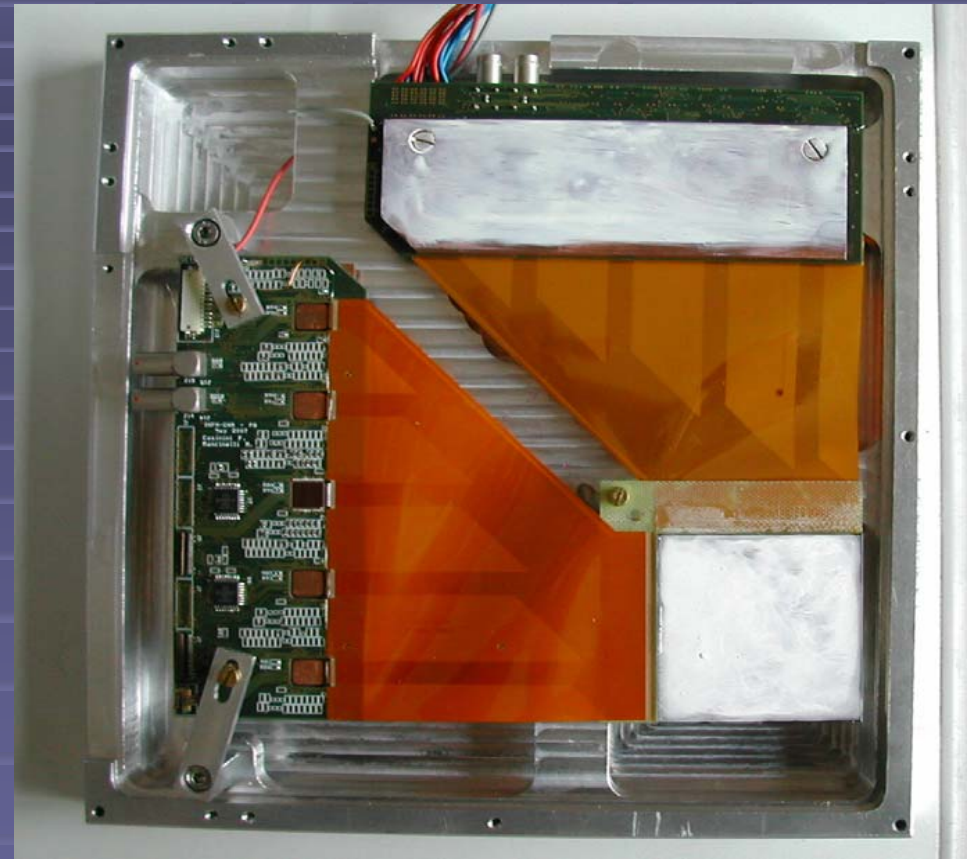
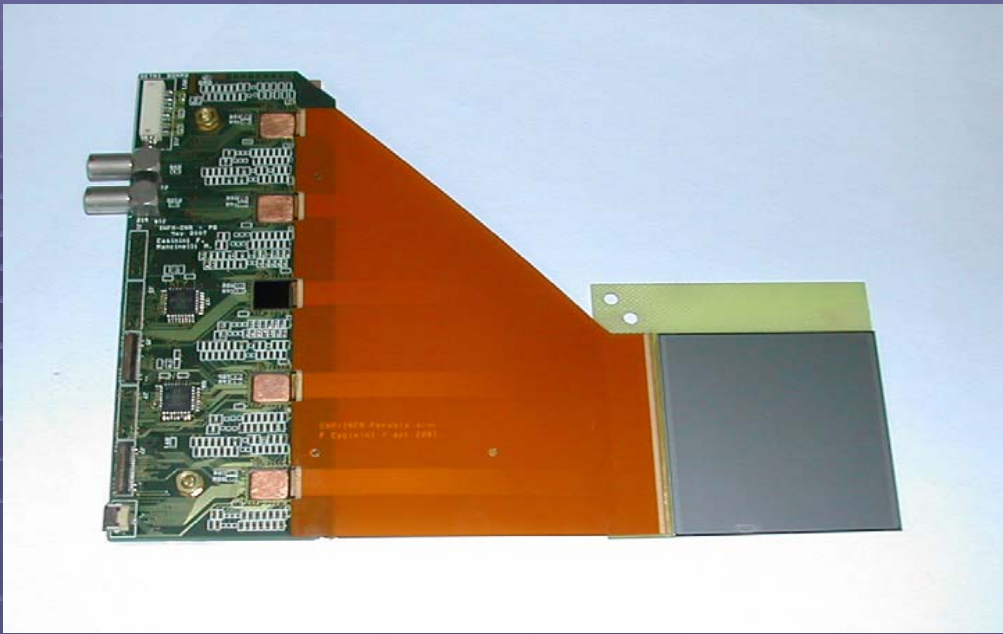
To dissipate the heat generated by ASICs a copper substrate to be connected to a liquid cooling system was designed.



ASICs bonding phase



# First prototype



Preliminary test in Berlin  
(unshielded readout  
electronics)



## Next steps

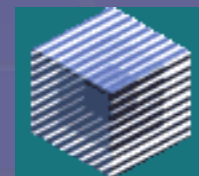
A readout test in collaboration with FZJ (who produced readout electronics) is scheduled for april 2009.

In the very first tests, a portable source (i.e.  $^{90}\text{Sr}$ ) will be used.

Once all eventual issues have been solved and the shielding system has been built, a neutron test will be performed .



Thanks for your attention



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